Joint CQSE and CASTS Seminar

Weekly Seminar
Nov. 17, 2017 (Friday)

TIME Nov. 17, 2017, 14:30 ~ 15:30
TITLE Epitaxial Ge/GeSn High Mobility Channel Transistors by CVD
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Abstract

To boost the drive current of transistor and/or reduce power consumption, new channel materials with high carrier mobility such as SiGe/Ge/GeSn have been considered as the promising candidates for the continuous scaling of Moore's law. SiGe channel have been used in the industry for pFETs, and the addition of Sn into Ge to further enhance the hole mobility is the attractive area of research. The strained GeSn on Ge/Si grown by CVD provides higher hole mobility than Ge due to the biaxial compressive strain and effective mass reduction by Sn incorporation.

To ensure the gate stack quality, and reduce the scattering of holes in the GeSn channel by oxide/interface charges and surface roughness, the epitaxy Ge cap with significant ΔE_V has been integrated. The Ge-cap/GeSn/Ge quantum well structure with [Sn] up to 9% is grown by CVD on SOI, and the low temperature process is used to fabricate the devices without Sn segregation/diffusion. By optimizing the cap thickness and thermal budget of gate stack formation, the high mobility (~430cm^2/V-s) of the CVD-grown GeSn quantum well p-MOSFETs is achieved to demonstrate the possible integration of GeSn material in industrial fabrication. The high hole mobility and reduced low frequency noise are obtained using quantum well structures with optimal cap thickness of 1 nm. The Ge cap also reduces the defects formed by Sn diffusion into dielectric. To improve the gate controllability and increase drive current with same footprint, the gate-all-around (GAA) pFETs using GeSn channels will be reported.

For Ge nFETs, junctionless GAAFETs with high drive current and high I_{on}/I_{off} are investigated. To boost the drive current and to suppress short channel effects, the optimized doping profile is needed. Since the subthreshold characteristic of JL FET is highly related to the channel cross-section and channel doping, the channel doping of $1.2x10^{19}cm^{-3}$ is used. However, it is too low for the S/D region, and heavily doped Ge (~$1.2x10^{20}$ cm^{-3}) is used in S/D by selective laser annealing with NiGe contact to reduce the parasitic resistance. The optimized doping profile is achieved by selective laser

annealing in the S/D, with Pt as hard mask on channel region to reflect the laser light in the channel. The demonstrated Ge JL nGAAFET with fin width (W_{fin}) down to 7 nm, EOT = 2.2 nm, and L_{ch} = 60 nm has I_{on} = 1146 μA/μm, I_{on}/I_{off} = 2×10^6, and SS = 95 mV/dec. The I_{on} can be further boost to 1235 μA/μm with external uniaxial tensile strain of 0.16%. The self-heating effect is responsible in part for such high I_{on}, because the high device temperature can reduce the dominant impurity scattering in the channel. Note that the increasing mobility with increasing temperature indicates the impurity scattering is dominant.

With Ge/GeSn CVD growth and optimized process, GAA transistors with high mobility channels can be realized as promising candidates for future CMOS scaling.